MIPS 70 μm Array Anomaly
ISA Z81711

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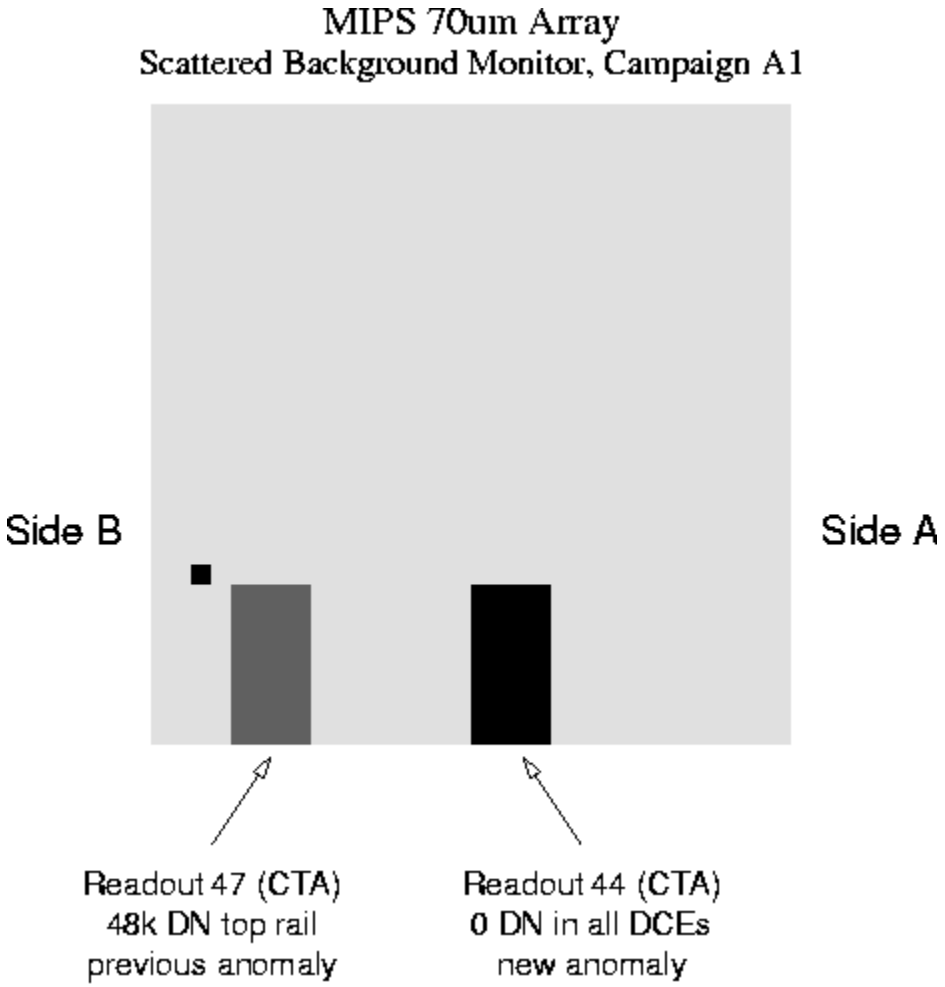
Description of Anomaly

- Problem discovered during MIPS aliveness testing in Campaign A1
  - Telescope temperature ~ 130 K was high enough to saturate all MIPS detectors
  - Aliveness test consisted of small changes in detector bias signals to drive detectors from rail to rail
  - Outputs of readout (4,4) (CTA convention) are stuck at negative rail.
  - Instrument telemetry shows no significant changes since ground test, indicating the array itself is healthy

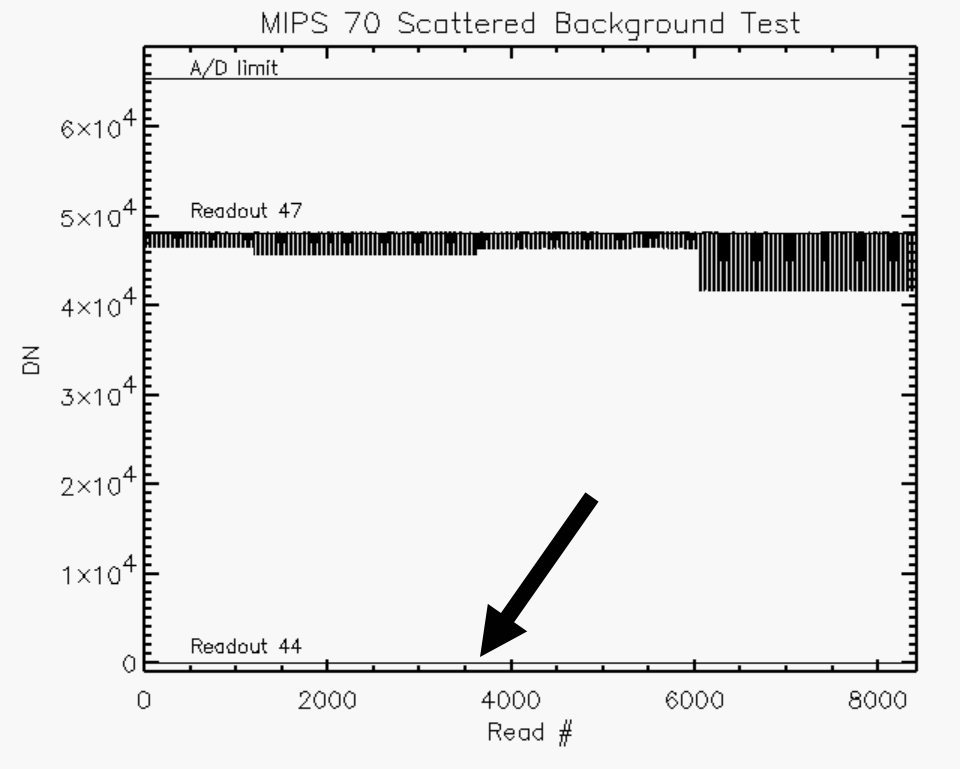
Pixel Map of 70 μm Array

- Majority of outputs behaved as expected.
- Readout (4,7) exhibited previously known short to ground. The 32 pixels from that readout have reduced amplitude.
- Readout (4,4) has output of 0 DN (negative rail) throughout the A1 campaign.

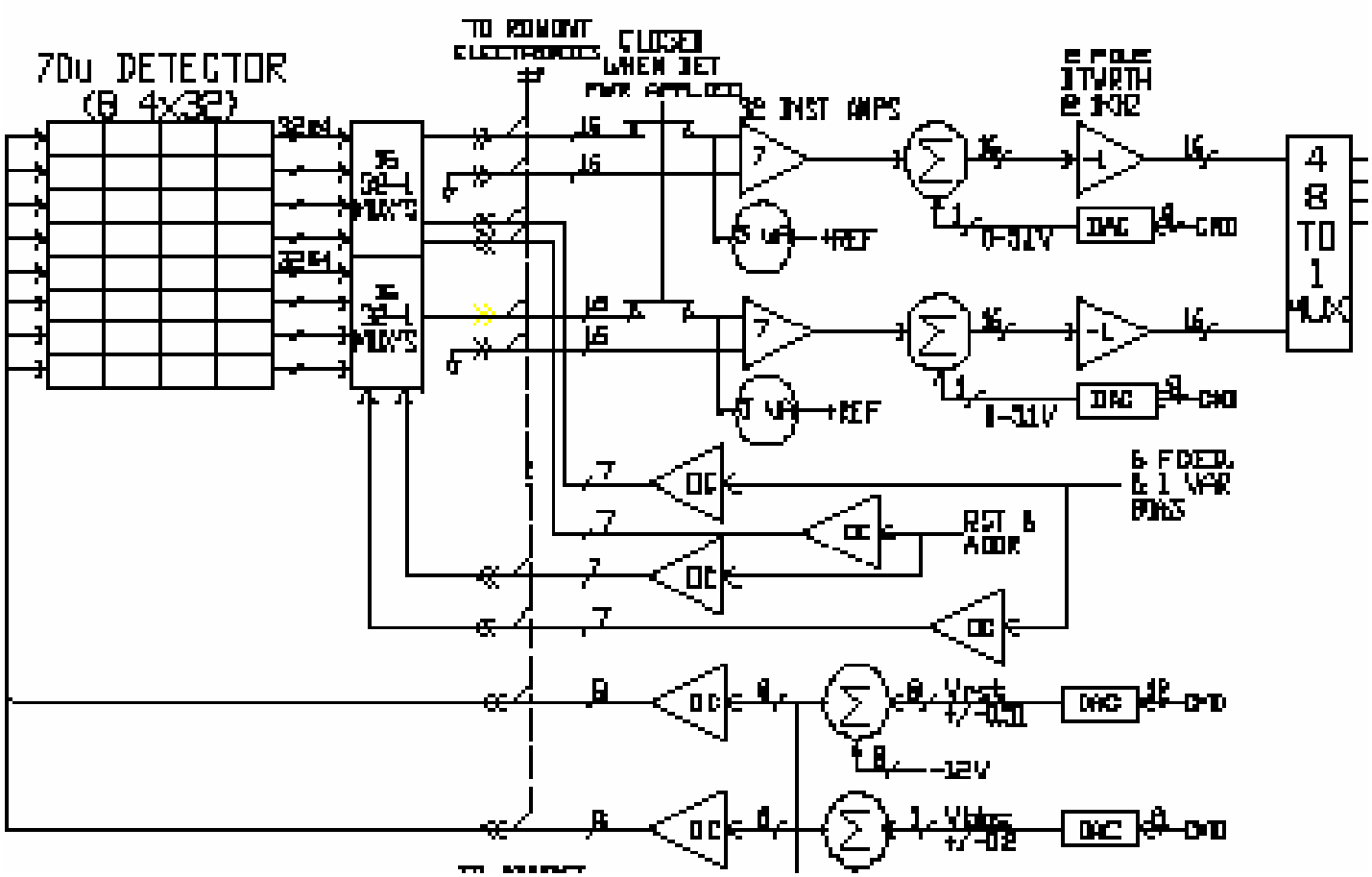


MIPS A1 Campaign DCE's

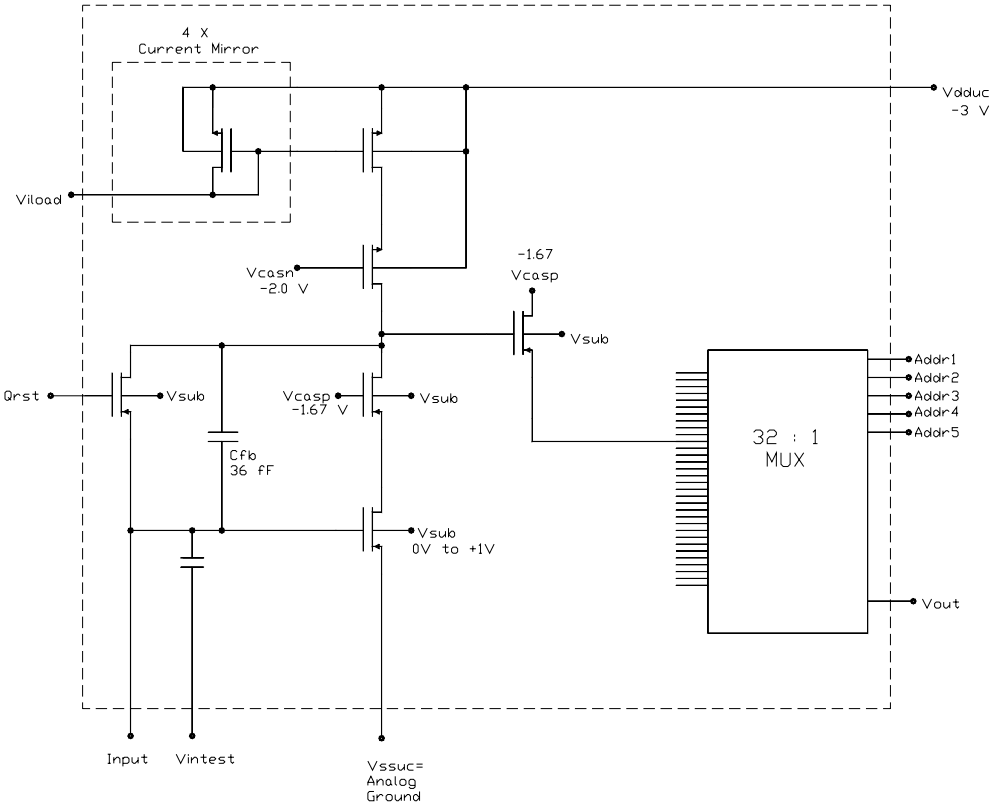
- (4,4) Pixel behavior unchanged throughout entire scattered background campaign



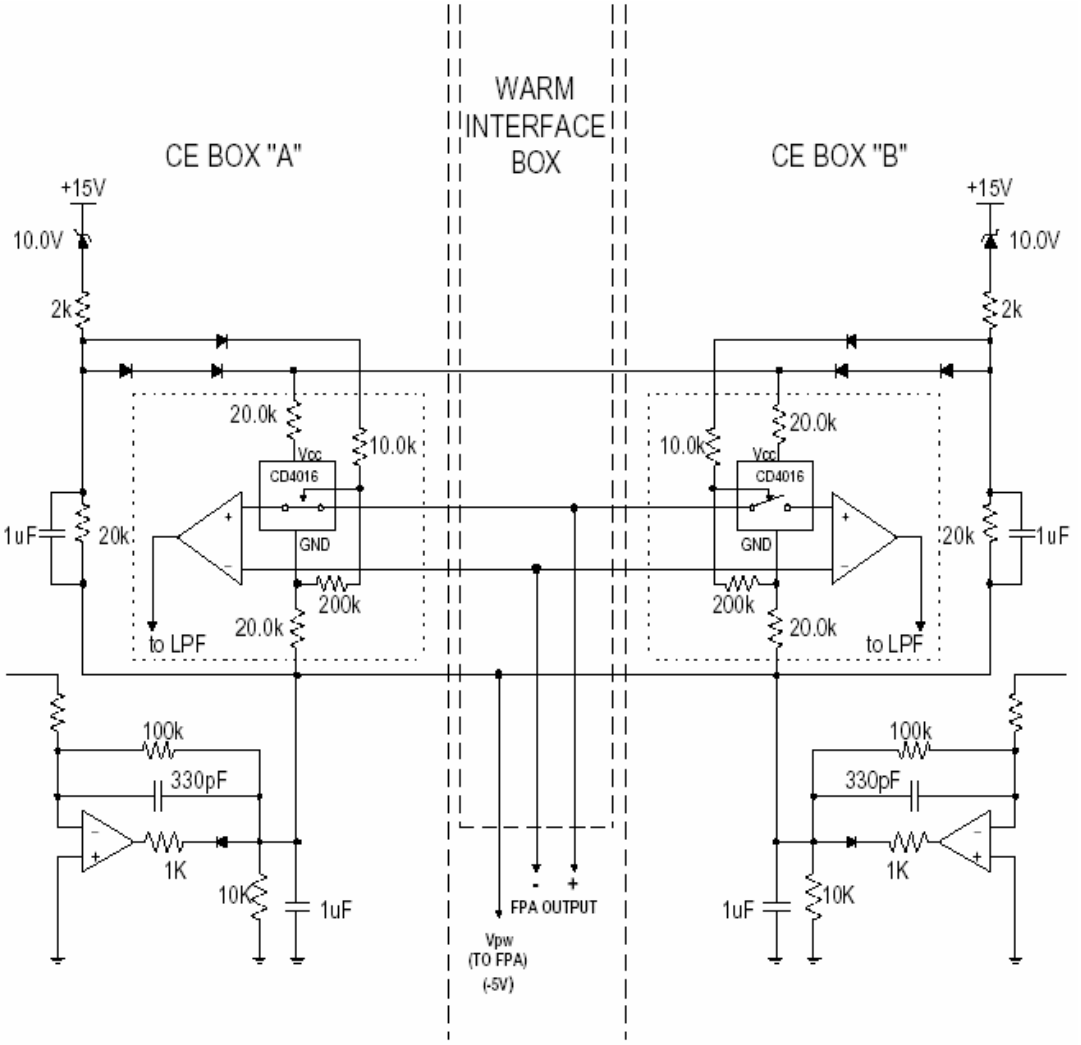
MIPS 70 μm Array Architecture



CRC-696 Schematic

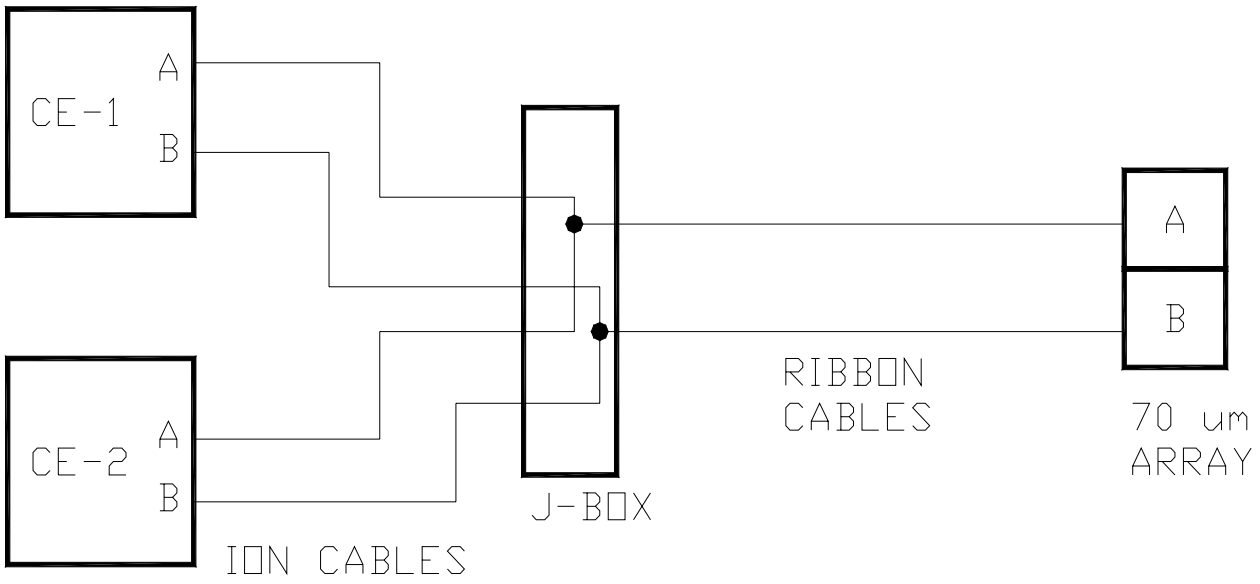


Differential Amplifiers



Cable Redundancy

- 70 μm array is divided into two identical 16x32 halves with non-redundant ribbon cables
- Cables to CE-1 and CE-2 warm electronics boxes are redundant after J-boxes.



Possible Causes

- Broken output line between readout and input of Combined Electronics
  - Each of the 32 outputs has a 5 μA constant current source
  - A broken output line will drive output to negative rail
  - We have previously encountered a broken line on the Side A CTA cryogenic cabling – that cable was replaced
- Failed wire bond at readout
- Failed readout chip
- Failed component in analog signal chain of CE prior to analog multiplexer
- Failure of specific input of analog multiplexer in CE

Ruled Out as Causes

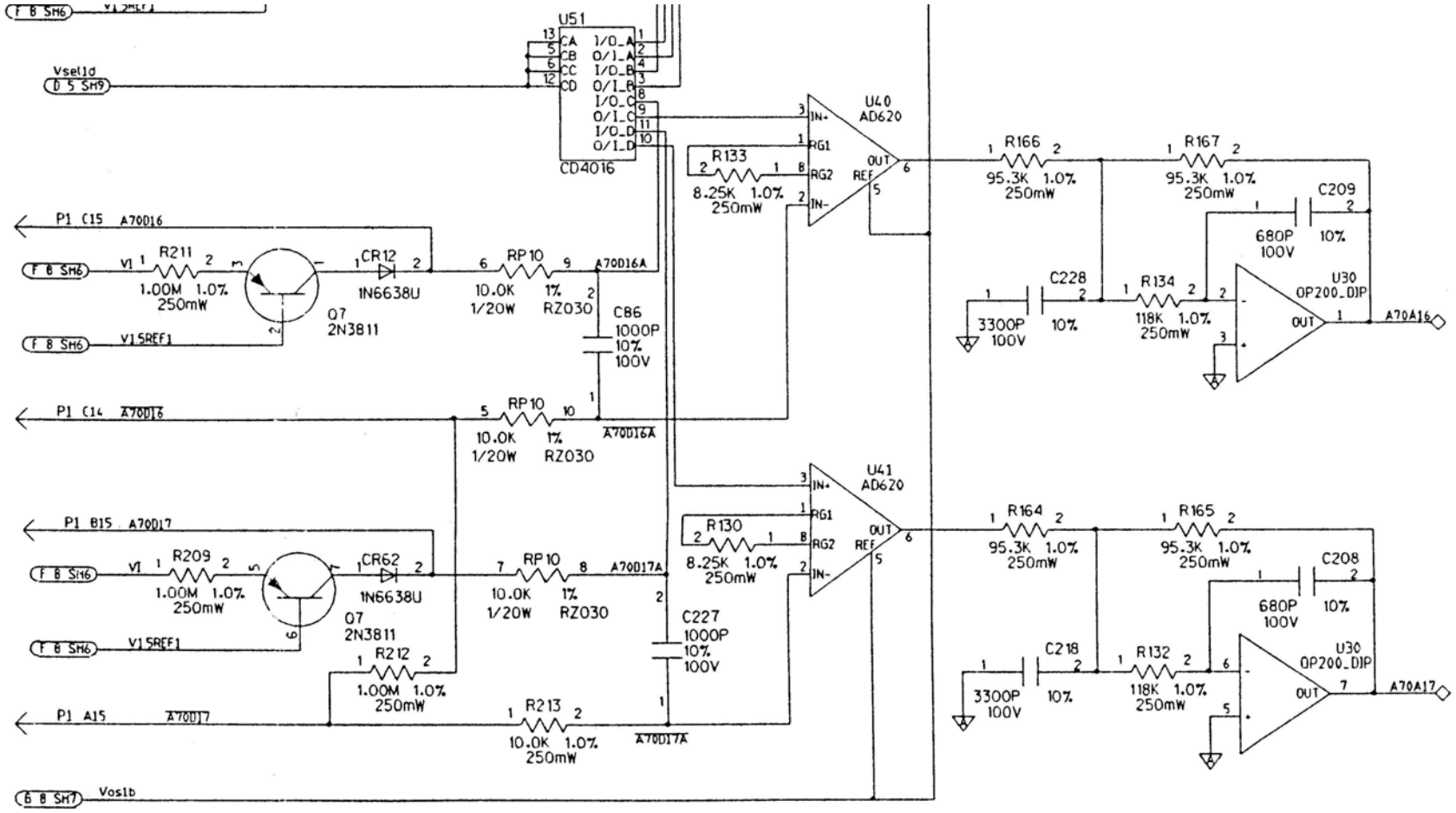
- Clock and Bias Drivers CE
  - Failure would affect half the array
- Clock and Bias Lines in Cables
  - Failure would affect half the array
- Clock and Bias Lines at Module Level
  - Failure would affect four readouts
- Output short to chassis
  - Would not drive output to negative rail
  - Observed fault would require a short to positive supply
- Open sense line for readout (4,4)
  - CE includes resistor to parallel sense line to guard against this possibility

Recommended Test

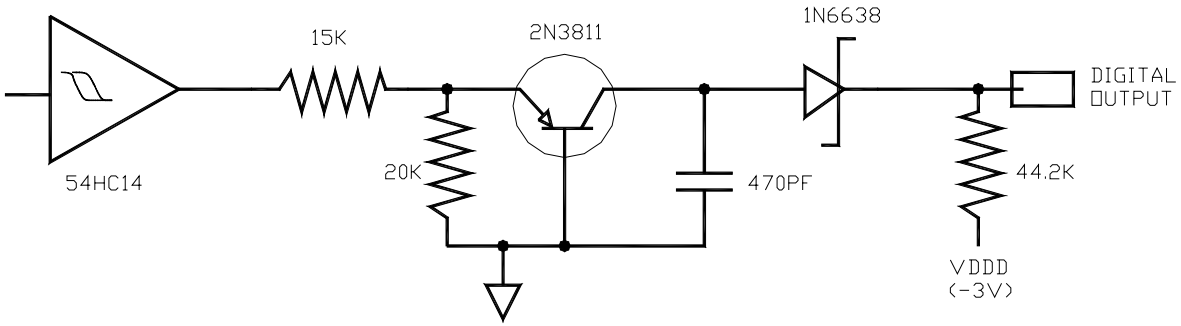
- We propose an engineering test that repeats the MIPS Campaign B with CE-2
  - If the fault is in the signal chain between the J-Box and the CE, the problem would be fixed
  - Any problem within the CE would also be fixed
  - Include variation of V_{offset} to diagnose open output line vs voltage shift
    - Initiated testing of IER
  - Anomaly team has focused on safety to the instrument
    - Most likely open circuit root cause poses no risk
    - MIPS was operated throughout Campaign A1 with no apparent effect to the other 31 readouts
    - Bias lines are current limited
    - Digital lines are current limited
  - No plausible additional risk to instrument has been identified
- Anomaly team has agreed that CE-1 remains the baseline electronics box

Backup Slides

CE 70 μm Input Stage



Typical Digital Driver



Typical Bias Driver